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TRANSMITTAL FORM

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Kathy Dixon

Box Patent Application
Assistant Commissioner
For Patents
Washington, D.C. 20231

Attorney Doc. #: 67.200-262
Mailing Date: June 6, 2000

Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): Heng-Ming Hsu Yen-Shih Ho

For: Planar Spiral Inductor Structure Having Enhanced Q Value

Submitted herewith are:

X 1 sheet of informal drawings showing Figs 1-3

X An Assignment of the invention to Taiwan Semiconductor Manufacturing Co., Ltd., together with Assignment Recordal Sheet

X A Declaration for patent application under CFR 1.63 and 1.68

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Small Entity Fee	Large Entity Fee	Total
Basic Fee			$345.00	$690.00	$690.00
Total Claims	15 x20	0 x	$9.00	$18.00	$0
Indep. Claims	2 -3	0 x	$39.00	$78.00	$0
Multiple Dep. Clms.			$130.00	$260.00	$0
Assign. Rec. Fee			$40.00	$40.00	$40.00
TOTAL					$730.00

Mailing Date: June 6, 2000
Attorney Docket No.: 67,200-262

_____ Please charge my Deposit Account No. _____ in the amount of $ _____. A duplicate copy of this sheet is enclosed.

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__X__ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0484. A duplicate copy of this sheet is enclosed.

__X__ Any additional filing fees required under 37 CFR 1.6
__X__ Any patent application processing fees under 37 CFR 1.17

Respectfully submitted,

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Enclosures

67,200-262
1999-545

PLANAR SPIRAL INDUCTOR STRUCTURE HAVING ENHANCED Q VALUE

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to co-assigned application serial number __/_____, filed ___ _____ 2000, attorney docket number 67,200-261, titled "Planar Spiral Inductor Structure With Patterned Interconnected Bond Pad Region Integral Thereto," the disclosure and references from which related co-assigned application are incorporated herein fully by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to inductor structures employed within microelectronic fabrications. More particularly, the present invention relates to planar spiral inductor structures employed within microelectronic fabrications.

2. Description of the Related Art

Microelectronic fabrications are fabricated from microelectronic substrates over which are formed patterned microelectronic conductor layers which are separated by microelectronic dielectric layers.

As microelectronic fabrication integration levels and functionality levels have increased, it has become common in the art of microelectronic fabrication to employ in addition to the generally conventional microelectronic device structures such as but not limited to transistor structures, resistor structures, diode structures and capacitor structures when fabricating microelectronic fabrications, less conventional microelectronic device structures such as inductor structures when fabricating microelectronic fabrications. In particular, within microelectronic fabrications which are intended to be employed within high frequency microelectronic fabrication applications, such as mobile communications high frequency microelectronic fabrication applications, it is often common to employ microelectronic inductor structures, in particular in conjunction with microelectronic capacitor structures, within those microelectronic fabrications.

While microelectronic inductor structures are thus desirable and often essential within the art of microelectronic fabrication, microelectronic inductor structures are nonetheless not entirely without problems in the art of microelectronic fabrication. In that regard, it is typically desirable in the art of microelectronic fabrication, but nonetheless not always readily achievable in the art of microelectronic fabrication, to fabricate microelectronic fabrications having formed therein microelectronic inductor structures with optimal properties, as characterized by enhanced Q values of the microelectronic inductor structures.

It is thus towards the goal of fabricating within microelectronic fabrications microelectronic inductor structures with optimal properties of the microelectronic inductor structures, as characterized by enhanced Q values of the microelectronic inductor structures, that the present invention is directed.

Various microelectronic inductor structures having desirable properties, including but not limited to enhanced Q values, have been disclosed in the art of microelectronic fabrication.

For example, Ashby et al., in "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process," IEEE J. of Solid State Circuits, Vol. 31(1), Jan. 1996, pp. 4-9, discloses a planar spiral inductor structure fabricated with a particularly enhanced Q value for use within a microelectronic fabrication. To realize the foregoing object, there is employed when fabricating the planar spiral inductor structure a substrate of higher substrate resistance and a spirally patterned conductor layer of lower series resistance.

In addition, Kitahara, in U.S. Patent No. 5,977,845 discloses a microelectronic inductor structure in conjunction with a microelectronic capacitor structure for use within a microelectronic fabrication, where there is avoided within the microelectronic inductor structure in conjunction with the microelectronic capacitor structure for use within the microelectronic fabrication a magnetic field effect upon the microelectronic capacitor structure as induced by the microelectronic inductor structure within the microelectronic fabrication. To realize the foregoing object, the microelectronic inductor structure comprises a pair of spiral inductor structures disposed geometrically with respect to the microelectronic capacitor structure such that a pair of magnetic fields generated by the pair of spiral inductor structures is equivalent, anti-parallel and cancels with respect to the microelectronic capacitor structure.

Finally, Yamazaki et al., in U.S. Patent No. 6,002,161, also discloses a planar spiral inductor structure fabricated with an enhanced Q value for use within a microelectronic fabrication. To realize the foregoing object, there is decreased when fabricating the planar spiral inductor

structure a series resistance of a spirally patterned conductor layer employed within the planar spiral inductor structure by employing within various portions of the spirally patterned conductor layer employed within the planar spiral inductor structure an additional laminated conductor layer which is insularly configured with respect to the spirally patterned conductor layer.

The teachings of the foregoing disclosures are incorporated herein fully by reference.

Desirable in the art of microelectronic fabrication are additional methods and materials which may be employed for fabricating within microelectronic fabrications microelectronic inductor structures with optimal properties, as characterized by enhanced Q values of the microelectronic inductor structures.

It is towards the foregoing object that the present invention is directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method for fabricating a microelectronic inductor structure within a microelectronic fabrication, as well as the microelectronic inductor structure fabricated within the microelectronic fabrication while employing the method.

A second object of the present invention is to provide a method and a microelectronic inductor structure in accord with the first object of the invention, wherein the microelectronic inductor structure is fabricated with optimal properties, as characterized by an enhanced Q value of the microelectronic inductor structure.

A third object of the present invention is to provide a method in accord with the first object of the present invention or the second object of the present invention, which method is readily commercially implemented.

In accord with the objects of the present invention, there is provided by the present invention a method for fabricating a microelectronic inductor structure within a microelectronic fabrication, as well as the microelectronic inductor structure which is fabricated within the microelectronic fabrication while employing the method.

To practice the method of the present invention, there is first provided a substrate. There is then formed over the substrate a planar spiral conductor layer to form a planar spiral inductor, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of: (1) a series of linewidths of the successive series of spirals; and (2) a series of spacings separating the successive series of spirals.

The method of the present invention contemplates a planar spiral inductor structure fabricated in accord with the method of the present invention.

The present invention provides a method for fabricating a microelectronic inductor structure within a microelectronic fabrication, as well as the microelectronic inductor structure fabricated within the microelectronic fabrication while employing the method, wherein the microelectronic inductor structure is fabricated with optimal properties, as characterized by an enhanced Q value of the microelectronic inductor structure. The present invention realizes the foregoing object by employing when fabricating a planar spiral inductor structure in accord with the present invention a spirally patterned conductor layer employed for forming the planar spiral inductor, where a successive series of spirals within the spirally patterned conductor layer is formed with a variation in at least one of: (1) a series of linewidths of the successive series of spirals; and (2) a series of spacings separating the successive series of spirals.

The method of the present invention is readily commercially implemented. As will become clear within the context of the Description of the Preferred Embodiment which follows, a microelectronic inductor structure fabricated in accord with the present invention may be fabricated employing methods and materials as are otherwise generally conventional in the art of microelectronic fabrication. Since it is largely structural features of a microelectronic inductor structure in accord with the present invention which provides at least in part the present invention, rather than the existence of methods and materials which provides the present invention, the method of the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

Fig. 1 shows a schematic plan view diagram of a microelectronic inductor structure fabricated in accord with the present invention.

Fig. 2 shows a schematic cross-sectional diagram of a microelectronic inductor structure corresponding with the microelectronic inductor structure whose schematic plan view diagram is illustrated in Fig. 1.

Fig. 3 shows a graph of Q versus Frequency for a microelectronic inductor structure fabricated in accord with the present invention, in comparison with an otherwise equivalent microelectronic inductor structure fabricated employing conventional linewidth and spacing dimensions.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for fabricating a microelectronic inductor structure within a microelectronic fabrication, as well as the microelectronic inductor structure fabricated within the microelectronic fabrication while employing the method, wherein the microelectronic inductor structure is fabricated with optimal properties, as characterized by an enhanced Q value of the microelectronic inductor structure. The present invention realizes the foregoing object by employing when fabricating a planar spiral inductor structure in accord with the present invention a spirally patterned conductor layer which comprises a successive series of spirals, and where the planar spiral conductor layer is formed with a variation of at least one of: (1) a series of linewidths of the successive series of spirals; and (2) a series of spacings which separate the successive series of spirals, within the spirally patterned conductor layer.

Although a microelectronic inductor structure fabricated in accord with the present invention provides particular value when fabricating an integrated circuit microelectronic fabrication which may be employed for higher frequency microelectronic fabrication applications, such as but not limited to wireless communications higher frequency microelectronic fabrication applications, a microelectronic inductor structure in accord with the present invention may be fabricated within a microelectronic fabrication selected from the group including but not limited to integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications, as employed within microelectronic fabrication applications including but not limited to higher frequency (i.e., greater than about 900 MHZ microelectronic fabrication applications, mid range frequency (i.e., from about 100 MHZ to

about 900 MHz microelectronic fabrication applications and lower frequency (i.e., less than about 100 MHZ) microelectronic fabrication applications.

Referring now to Fig. 1 there is shown a schematic plan view diagram of a microelectronic inductor structure fabricated in accord with a preferred embodiment of the present invention.

Shown in Fig. 1 is a substrate 10 having formed thereupon a spirally patterned conductor layer 12, where the spirally patterned conductor layer 12 has a series of spirals which is formed with a variation of linewidths within the series of spirals within the spirally patterned conductor layer 12. Within the schematic plan view diagram of Fig. 1, the spirally patterned conductor layer 12 forms a planar spiral inductor structure in accord with the present invention. As will be illustrated more particularly within the context of the examples which follow, by employing when forming the spirally patterned conductor layer 12 the series of spirals with the variation in linewidths, there is provided within the context of the present invention a planar spiral inductor structure with optimal properties, as characterized by an enhanced Q value of the planar spiral inductor structure.

As is illustrated within the schematic plan-view diagram of Fig. 1, a microelectronic inductor structure of the present invention which is formed as the planar spiral inductor structure of the present invention is formed of a bidirectional outer spiral width W1 of from about 250 to about 400 microns which defines an outer periphery of the planar spiral inductor structure, while similarly having a bidirectional inner spiral width W2 of from about 30 to about 120 microns which defines

an inner cavity within the center of the planar spiral inductor structure of the present invention. As is illustrated within the schematic plan view diagram of Fig. 1, when forming a series of spirals within the preferred embodiment of the planar spiral inductor structure of the present invention, a linewidth of each of the spirals which comprises the series of spirals within the spirally patterned conductor layer 12 which forms the planar spiral inductor structure of the present invention becomes progressively wider as the series of spirals progress from the innermost spiral to the outermost spiral. Typically and preferably, the linewidth progresses from: (1) a most narrow linewidth LW1 of from about 7 to about 10 microns for an innermost spiral, to; (2) a less narrow linewidth LW2 of from about 10 to about 13 microns for a more inner interior spiral, to; (3) a still less narrow linewidth LW3 of from about 13 to about 17 microns for a more outer interior spiral, to; (4) a widest linewidth LW4 of from about 17 to about 21 microns for an outermost spiral.

Although the preferred embodiment and examples of the present invention illustrate the present invention within the context of a progressive and discontinuous variation of linewidth within a series of spirals within a planar spiral inductor structure in accord with the present invention, in a more broad sense, the present invention seeks to enhance electrical and electromagnetic properties of planar spiral inductor structures employed within microelectronic fabrications, and in particular to provide optimal properties within a planar spiral inductor structure as characterized by an enhanced Q value within the planar spiral inductor structure, by adjusting by means of variations including but not limited to continuous variations and discontinuous variations at least one of: (1) a series linewidths of a successive series of spirals; and (2) a series of spacings separating the successive series of spirals, within a spirally patterned conductor layer within a planar

spiral inductor structure when fabricating the planar spiral inductor structure in accord with the present invention. Thus, the present invention is not strictly limited to the particular linewidths variation within a successive series of spirals within a spirally patterned conductor layer when fabricating a planar spiral inductor structure as is illustrated within the preferred embodiment of the present invention or the examples of the present invention. Rather, the present invention may also include alternative linewidths variation and/or spacings variation within a series of spirals within a spirally patterned conductor layer within a planar spiral inductor structure which effect similar and related results to those as disclosed within the preferred embodiment and examples of the present invention. Such specific and alternative linewidths variation and spacings variation which provide optimal performance of a planar spiral inductor structure in accord with the present invention are not believed to require undue experimentation for their discovery, insofar as a planar spiral inductor structure is a comparatively simple microelectronic device structure which is typically fabricated while employing a single etch mask layer which may be employed for forming a series of spirals within a spirally patterned conductor layer within the planar spiral inductor structure.

Similarly, although the schematic plan view diagram of Fig. 1 illustrates the planar spiral inductor structure of the present invention as being formed employing three and one half full spirals in a nominally rectangular geometry for the planar spiral inductor structure of the preferred embodiment of the present invention, planar spiral inductor structures in accord with the present invention may be formed employing geometries including but not limited to triangular geometries, square geometries, rectangular geometries, higher order polygonal geometries, uniform elliptical geometries, non-uniform elliptical geometries and circular geometries having a number of spirals ranging from about 2 to about 8.

Referring now to Fig. 2, there is shown a schematic cross-sectional diagram of a microelectronic inductor structure corresponding with the microelectronic inductor structure whose schematic plan view diagram is illustrated in Fig. 1.

Similarly within microelectronic inductor structure whose schematic plan view diagram is illustrated in Fig. 1, there is shown within the microelectronic inductor structure whose schematic cross-sectional diagram is illustrated in Fig. 2 the substrate 10 having formed thereupon a series of spirally patterned conductor layers 12a, 12b, 12c, 12d, 12d', 12c', 12b' and 12a' which derive from the spirally patterned conductor layer 12 as illustrated within the schematic plan view diagram of Fig. 1, and where the linewidths LW1, LW2, LW3 and LW4 of the series of spirally patterned conductor layers 12a, 12b, 12c, 12d, 12d', 12c', 12b' and 12a' correspond with the linewidths LW1, LW2, LW3 and LW4 of the spirally patterned conductor layer 12 as illustrated within the schematic plan view diagram of Fig. 1.

Within the preferred embodiment of the present invention with respect to the substrate 10, the substrate 10 may be employed within a microelectronic fabrication selected from the group including but not limited to integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications, although, as noted above, a planar spiral inductor structure in accord with the present invention is most likely to provide value when fabricating an integrated circuit

microelectronic fabrication which is employed within a higher frequency microelectronic fabrication application, such as a wireless communication higher frequency microelectronic fabrication application.

Although not specifically illustrated in the schematic cross-sectional diagram of Fig. 2, the substrate 10 may consist of a substrate alone as employed within the microelectronic fabrication, or in an alternative, the substrate 10 may comprise the substrate as employed within the microelectronic fabrication, where the substrate has formed thereupon and/or thereover any of several additional microelectronic layers as are conventionally employed within the microelectronic fabrication within which is employed the substrate 10. Similarly with the substrate alone as employed within the microelectronic fabrication, such additional microelectronic layers may be formed of microelectronic materials including but not limited to microelectronic conductor materials, microelectronic semiconductor materials and microelectronic dielectric materials.

Similarly, although also not specifically illustrated within the schematic cross-sectional diagram of Fig. 2, the substrate 10, typically and preferably, but not exclusively, when the substrate 10 consists of or comprises a semiconductor substrate employed within a semiconductor integrated circuit microelectronic fabrication, has formed therein and/or thereupon microelectronic devices as are conventional within the microelectronic fabrication within which is employed the substrate 10. Such microelectronic devices may include, but are not limited to, transistors, resistors, diodes and capacitors.

Most preferably, although not exclusively, within the preferred embodiment of the present invention the substrate 10: (1) comprises a semiconductor substrate employed within a semiconductor integrated circuit microelectronic fabrication; (2) the semiconductor substrate has formed therein and/or therupon microelectronic devices as are conventional within the semiconductor integrated circuit microelectronic fabrication within which is employed the semiconductor substrate; and (3) the top surface of the substrate 10 is formed of an integrated circuit microelectronic layer formed of a dielectric material.

Within the preferred embodiment of the present invention with respect to the series of spirally patterned conductor layers 12a, 12b, 12c, 12d, 12d', 12c', 12b' and 12a', the series of spirally patterned conductor layers 12a, 12b, 12c, 12d, 12d', 12c', 12b' and 12a' may be formed from any of several conductor materials as are conventional in the art of microelectronic fabrication for forming inductor structures or conductor structures within microelectronic fabrications, such conductor materials being selected from the group including but not limited to: (1) non-magnetic metal and non-magnetic metal alloy (such as but not limited to aluminum, aluminum alloy, copper and copper alloy) conductor materials: (2) magnetic metal and magnetic metal alloy (such as permalloy and higher order alloys incorporating permalloy alloy) conductor materials; (3) doped polysilicon (having a dopant concentration greater than about 1E18 dopant atoms per cubic centimeter) and polycide (doped polysilicon/.metal silicide stack) conductor materials; and (4) laminates thereof. Typically and preferably, each of the spirally patterned conductor layers 12a, 12b, 12c, 12d, 12d', 12c', 12b', and 12a' is formed to a thickness of from about 4000 to about 35000 angstroms.

Upon forming the microelectronic fabrication whose schematic plan view diagram is illustrated in Fig. 1 and whose schematic cross-sectional diagram is illustrated in Fig. 2, there is formed a microelectronic fabrication having formed therein a microelectronic inductor structure with optimal properties, as characterized by an enhanced Q value of the microelectronic inductor structure. The present invention realizes the foregoing object by fabricating the microelectronic inductor structure of the present invention as a planar spiral inductor structure, wherein a series of spirals within the planar spiral inductor structure is formed with a variation in at least one of: (1) a series linewidths of the successive series of spirals; and (2) a series of spacings separating the successive series of spirals.

EXAMPLES

In order to illustrate the value of the present invention, there was fabricated as a first example a planar spiral inductor structure generally in accord with the planar spiral inductor structure whose schematic plan view diagram is illustrated in Fig. 1 and whose schematic cross-sectional diagram is illustrated in Fig. 2, but wherein there was employed a total of five spirals within the planar spiral inductor structure rather than the three and one half spirals within the planar spiral inductor structure whose schematic plan view diagram is illustrated in Fig. 1. The five spirals progressed from a most narrow linewidth spiral within the center of the planar spiral inductor structure to a most wide linewidth spiral at the periphery of the planar spiral inductor structure. The linewidths of the spirals progressed in the order of about 9 microns, to about 12 microns, to about 15 microns, to about 18 microns and finally to about 21 microns. Each of the spirals was separated by a spacing (i.e., pitch) dimension of about 1.5 microns. Similarly, an inner cavity of the planar

spiral inductor structure was defined by a bidirectional cavity width of about 120 microns and an outer periphery of the planar spiral inductor structure was defined by a bidirectional linewidth of about 280 microns. Finally, each of the spirals within the planar spiral inductor structure was formed to a thickness of about 20000 angstroms from an aluminum alloy conductor material.

For comparison, purposes, there was also fabricated as a second example a more conventional planar spiral inductor structure otherwise generally equivalent with the planar spiral inductor structure fabricated in accord with the first example, but wherein each spiral within the series of five spirals had a linewidth of about 15 microns, rather than the variable linewidth as disclosed above.

Each of the two planar spiral inductor structures in accord with the examples was then electrically tested employing electrical testing methods as are conventional in the art of microelectronic fabrication. For both of the planar spiral inductor structures in accord with the examples, there was observed no discernable variation in a resonant frequency of about 8 Ghz. However, with respect to measurement of Q value as a function of frequency, it is seen, by reference of the graph of Fig. 3, that at frequencies of greater than about 1.5 gigahertz there is approximately a 20 percent increase in Q value for a planar spiral inductor structure fabricated in accord with the present invention and further in accord with the first example, as characterized by the curve corresponding with reference numeral 14, in comparison with a planar spiral inductor structure more conventionally fabricated in accord with the second example, as characterized by the curve

curve corresponding with reference numeral 16. For reference purposes, specifics of calculation of Q values are provided within Yamazaki, U.S. Patent No. 6,002,161, within the Description of the Related Art.

Thus, in accord with the examples of the present invention, it is clear that the present invention and the preferred embodiment of the present invention provide within a microelectronic fabrication a microelectronic inductor structure with optimal properties, as characterized by an enhanced Q value of the microelectronic inductor structure.

As is understood by a person skilled in the art, the preferred embodiment and examples of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials, structures and dimensions through which is fabricated within a microelectronic fabrication in accord with the preferred embodiment of the present invention a microelectronic inductor structure while still fabricating a microelectronic fabrication having fabricated therein a microelectronic inductor structure in accord with the present invention, further in accord with the appended claims.

What is claimed is:

1. A method for fabricating an inductor structure comprising:

providing a substrate;

forming over the substrate a planar spiral conductor layer to form a planar spiral inductor, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of:

a series of linewidths of the successive series of spirals; and

a series of spacings separating the successive series of spirals.

2. The method of claim 1 wherein by employing within the successive series of spirals within the planar spiral conductor layer the variation in at least one of the series of linewidths of the successive series of spirals and the series of spacings separating the successive series of spirals, the planar spiral inductor is fabricated with an enhanced Q value.

3. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

4. The method of claim 1 wherein the successive series of spirals is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, a uniform ellipse, a non-uniform ellipse and a circle.

5. The method of claim 1 wherein the planar spiral conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

6. The method of claim 1 wherein the variation in the series of linewidths of the successive series of spirals is an increasing progression of linewidth from a first spiral which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final spiral which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

7. The method of claim 6 wherein the comparatively narrow linewidth is from about 7 to about 10 microns and the comparatively wide line width is from about 17 to about 21 microns.

8. The method of claim 1 wherein the successive series of spirals comprises from about 1 to about 8 spirals.

9. An inductor structure comprising:

a substrate;

a planar spiral conductor layer formed over the substrate to form a planar spiral inductor formed over the substrate, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of:

a series of linewidths within the successive series of spirals; and

a series of spacings separating the successive series of spirals.

10. The inductor structure of claim 9 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

11. The inductor structure of claim 9 wherein the successive series of spirals is formed in a shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, a uniform ellipse, a non-uniform ellipse and a circle.

12. The inductor structure of claim 9 wherein the planar spiral conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

13. The inductor structure of claim 9 wherein the variation in the series of linewidths of the successive series of spirals is an increasing progression of linewidth from a first spiral which defines the center of the planar spiral inductor having a comparatively narrow linewidth to a final spiral which defines the perimeter of the planar spiral inductor having a comparatively wide linewidth.

14. The inductor structure of claim 13 wherein the comparatively narrow linewidth is from about 7 to about 10 microns and the comparatively wide line width is from about 17 to about 21 microns.

15. The inductor structure of claim 9 wherein the series of spirals comprises from about 1 to about 8 spirals.

PLANAR SPIRAL INDUCTOR STRUCTURE HAVING ENHANCED Q VALUE

ABSTRACT OF THE DISCLOSURE

Within a method for fabricating an inductor structure there is first provided a substrate. There is then formed over the substrate a planar spiral conductor layer to form a planar spiral inductor, wherein a successive series of spirals within the planar spiral conductor layer is formed with a variation in at least one of: (1) a series of linewidths of the successive series of spirals; and (2) a series of spacings of the successive series of spirals. The method contemplates a planar spiral inductor structure fabricated in accord with the method. A planar spiral inductor structure fabricated in accord with the method is characterized by an enhanced Q value of the planar spiral inductor structure.

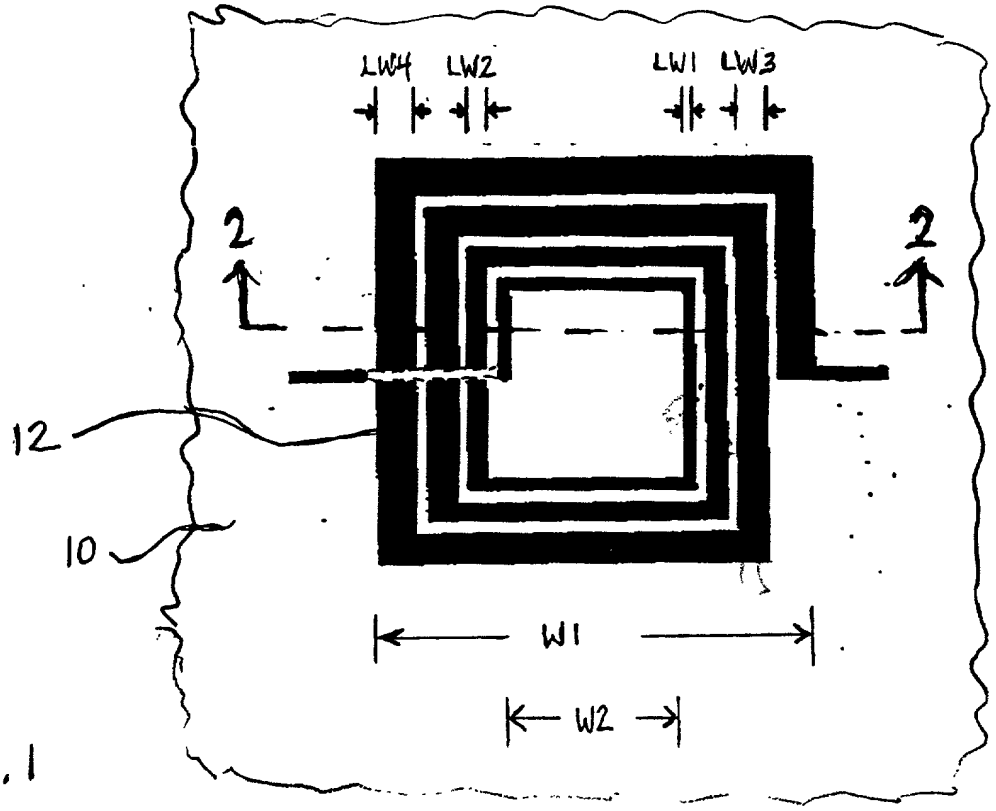

Fig. 1

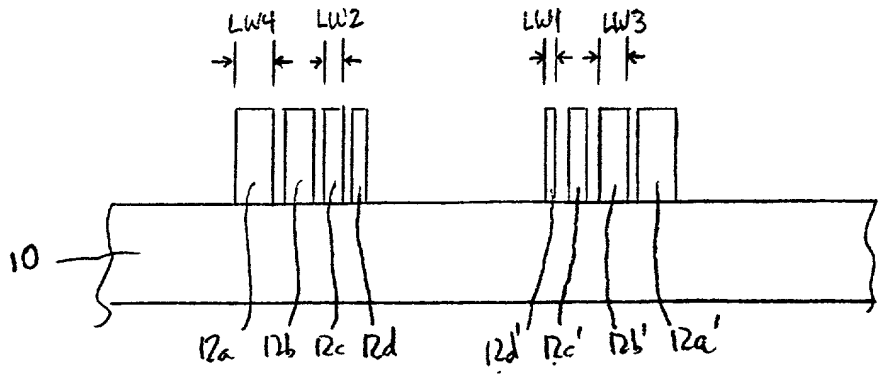

Fig. 2

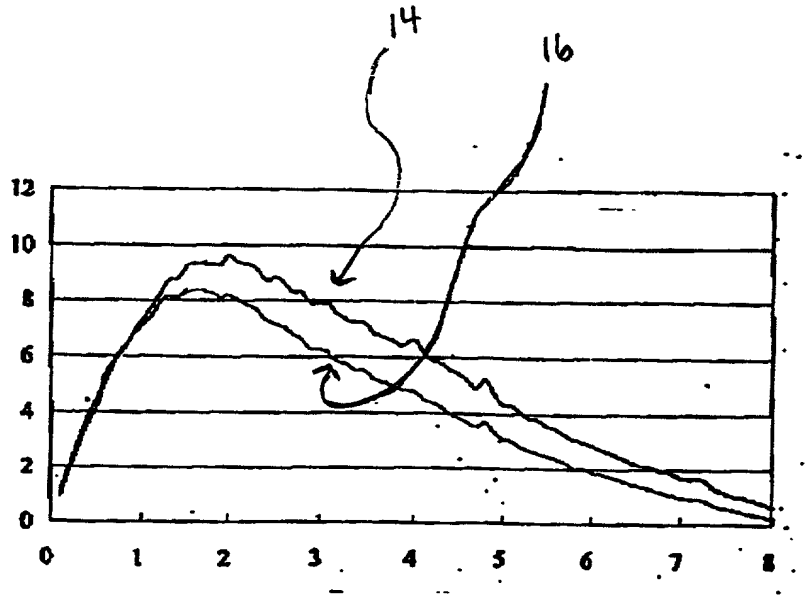

Fig. 3

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DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "PLANAR SPIRAL INDUCTOR STRUCTURE HAVING ENHANCED Q VALUE" the specification of which

__X__ is attached hereto.
_____ was filed on _____ as
Application Serial No. _____
And was amended on _____
(If applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendments referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56, a copy of which is attached.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent on inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			**Priority Claimed**	
Number	Country	Day/Month/Year	(Yes)	(No)
Number	Country	Day/Month/Year	(Yes)	(No)
Number	Country	Day/Month/Year	(Yes)	(No)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Ser. No.	Filing Date	Status
Application Ser. No.	Filing Date	Status

I further declare that I do not know and do not believe that the invention claimed in this application was ever known or used by others in this country before my invention thereof, or patented or described in any printed publication in any country before my invention thereof, or more than one year prior to this application or any prior U.S. application above identified in which said invention may have been disclosed, or in public use or on sale in the United States of America for more than one year prior to this application or any prior U.S. application above identified in which said invention may have been disclosed.

POWER OF ATTORNEY

And I hereby appoint as my attorneys with full power of substitution to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith to the firm of **TUNG & ASSOCIATES,** including the following individual attorneys associated with the firm:

Individual Attorneys	**Reg. No.**
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and of any patent issued thereon.

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§1.56 Duty to disclose information material to patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application; and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.

(35 U.S.C. 6, Pub. L. 97-247)

[42 FR 5593. Jan. 28, 1977, as amended at 47 FR 21751, May 19, 1982; 48 FR 2710, Jan. 20, 1983; 49 FR 554, Jan. 4, 1984; 50 FR 5171, Feb. 6, 1985; 53 FR 47808, Nov. 28, 1988, effective Jan. 1, 1989; 57 FR 2034, January 17, 1992, effective March 6, 1992]